RC6516

IF Demodulator for Vestigial Side Band Receivers

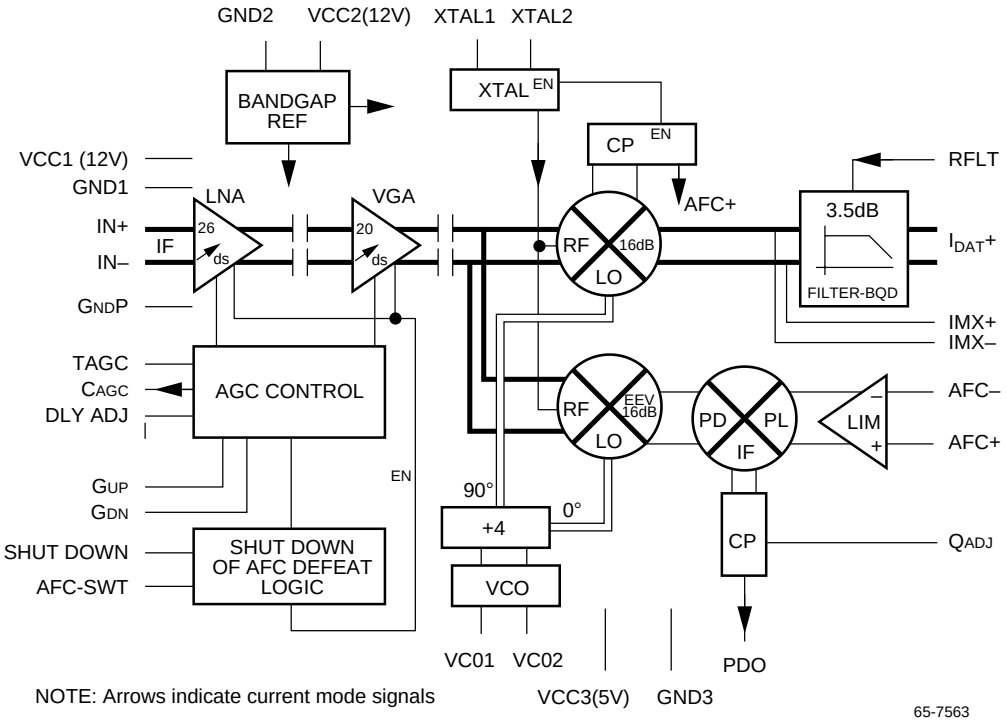
Features

- Demodulates 16 level to 2 level VSB signals
- Versatile delayed AGC & Tuner Controls
- 60dB Gain from IF to baseband
- 45dB AGC range with a digital control
- <1% distortion @ 2 Vpp baseband output
- 50dB typical IMD3
- On-chip low phase noise VCO (100dBc/Hz @ 20KHz from 200MHz)
- Wideband Quadrature Prescalers
- <2° Quadrature phase error
- Programmable Video Filter-Amplifier
- Direct input interface for SAW filters
- 9dB input Noise Figure at max gain
- On-chip band gap reference and temperature compensation
- Available in 28 lead PLCC package

Description

The RC6516 is fully integrated IF Demodulator customized for Vestigal Side Band (VSB) receivers. As shown in the Block Diagram, the IC performs IF amplification with gain control, synchronous demodulation of I & Q channels and carrier recovery using a Frequency & Phase Lock Loop (FPLL). The RC6516 directly provides delayed AGC control for a front end tuner. The demodulated output is filtered and amplified. The device accepts direct digital control inputs from a microprocessor for gain control, calibration and shut down functions. The IC is packaged in a 28-pin PLCC.

Block Diagram



Rev. 0.9.0

Functional Description

The block diagram of the RC6516 consists of three general sections:

1. IF amplifiers with gain control
2. Synchronous demodulator
3. Frequency phase lock loop (FPLL) and auxiliary circuits

The IF Section

There are two IF amplifiers capacitatively coupled to each other and the subsequent stages. The first amplifier has a maximum gain of 24dB and an AGC range of more than 14dB. The second amplifier has a maximum gain of 16dB and gain reduction capability of 30dB. To minimize the Noise Figure degradation with gain reduction the second stage fully gain reduces before the first stage gain reduces. The transition point is set by the voltage on the DLYADJ pin. The voltage on CAGC pin directly determines the gain of the two IF stages. When the voltage on CAGC is lower the IF gain is lower. When the CGAC voltage is higher than the DLYADJ the gain reduction is primarily in the second stage. When the CAGC voltage is lower than DLYADJ, only the first stage gain is reduced at a much slower rate. The tuner AGC control voltage TAGC also changes this range to gain reduce the external tuner. This avoids the amplifiers from being overdriven into distortion. During AFC defeat mode these IF amplifiers are disabled with more than 50dB of signal isolation.

Gain Control

The gain control signal is developed on the capacitor at the CAGC pin, by charge pump and AGC control circuits. TTL/CMOS signals on the G_{UP}, G_{DN} pins build the voltage through the charge pump current at CAGC pin. Continuous pulses on GUP pin increases the CAGC voltage and pulses on the GDN pin reduces the CAGC voltage. Table 1 shows the truth table for gain control.

Synchronous Demodulator

This section consists of In-phase (I) and Quadrature (Q) multipliers/mixers.

During normal operation the incoming signal processed by the two IF stages is capacitatively coupled to the linear (RF) port of both the mixers. The signals for the LO port of the I & Q mixers come from the FPLL section. The switching signals are in quadrature and phase locked to a small pilot present in the IF signal. The signal levels for this multiplying port use limiting amplitudes. The I channel output is then filtered to reject the high frequency components while not distorting the video band signals. The filtered output is also amplified to cover the full range of A/D converter that follows. The Q channel signal is used by the FPLL section described below.

The FPLL Section

The FPLL consists of a VCO working at 4 times the pilot frequency. The frequency is set by external LC components and also controlled with a varactor. This VCO signal is passed through a divide by 4 prescaler to provide two signals in quadrature at the frequency of the pilot. These signals are used by the I & Q multipliers. The VCO is frequency and phase locked to the 4x pilot frequency which is typically 46.69MHz. The VCO thus operates at 186.7MHz in a typical 16 VSB decoder. Frequency acquisition is possible by means of the third multiplier on chip and AFC filter off-chip. The PLL circuit is formed by the Q channel mixer, third multiplier-charge pump, external PLL filter and the VCO.

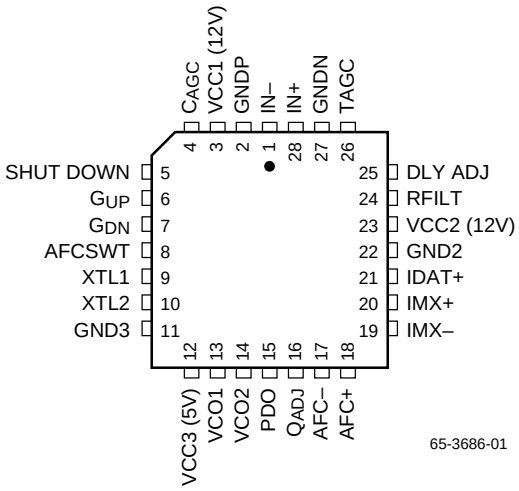
Due to component variations, the VCO frequency may not be within the pull in range of the FPLL. The AFCSW signal is used for activating this start up calibration. An auxiliary crystal oscillator signal at the pilot frequency of 46.6MHz is injected into the input port of the mixers, to pull the VCO to the desired frequency during the start up mode. During this mode the XTAL oscillator and the I-channel charge pump are activated and the IF gain stages are disabled. There is also the shutdown mode during which the VCO, the crystal oscillator and the tuner control are disabled. These various states are determined as shown in Table 1.

Table 1. Truth Table for Digital Circuitry

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, T_A = 0 to 70°C unless otherwise specified

AGC Control		
G_{UP}	**G_{DN}**	**Description**
LO	LO	No Gain Change (over symbol period)
HI	LO	Increase Gain
LO	HI	Decrease Gain
HI	HI	Disallowed
AFC Control		
AFC_SWT	**SHTDWN**	**Description**
LO	LO	Crystal is OFF, VCO is ON
X	HI	Crystal is OFF, VCO is OFF, Tuner AGC is Hi-Z
HI	LO	Crystal is ON, VCO is on, I-channel Charge Pump is ON for acquisition

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
AFC+, AFC–	18, 17	Inputs to the limiter that sets the polarity of the third multiplier in the FPLL loop.
AFCSWT	8	This digital input is LO during normal operation. A TTL/CMOS high input enable the crystal oscillator and an extra I-channel charge pump, while disabling the IF input sections. The crystal oscillator outputs are switched into the input ports of the quadrature mixers. The VCO then locks to 4 x crystal frequency.
C_{AGC}	4	An internal charge pump will develop a voltage across any capacitance on this pin. Voltage on this node directly determines the front end IF gain. When operating on a 12 volt supply, moving this voltage from 9V to 2V reduces the gain by at least 40dB.
DLYADJ	25	The input voltage on this pin determines the transition point for delayed AGC.
G_{DN}	7	A TTL/CMOS high level input on this pin activates internal charge up to decrease the voltage on the CAGC pin.
GND2	22	Ground line for backend. Also the substrate connection to the IC. Should be at the lowest potential to the IC.
GND3	11	Ground line for digital section.
GNDN	27	Shield ground for input.
GNDP	2	Ground signals for front end sections.
G_{UP}	6	A TTL/CMOS high level input on this pin activates internal charge up to increase the voltage on the CAGC pin.
IDAT+	21	Demodulated & filtered output to be ac coupled to A/D converter.
IMX+, IMX–	20, 19	Demodulated output before filtering. DC coupled back to AFC limiter inputs AFC+/AFC– though an external low pass filter.
IN+, IN–	28, 1	IF inputs to be demodulated. Internal dc restoration. External ac coupling required. Usually interfaced to a SAW filter.
PDO	15	Charge pump output from third multiplier. This output can be fed to an external lead-lag filter to develop the voltage required to drive the varactor in feedback till a lock is established with the pilot.

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Pin Descriptions (continued)

Pin Name	Pin Number	Description
QADJ	16	Offset adjust input pin effectively corrects quadrature phase error. A 20KΩ variable resistor to ground can cover the range of correction.
RFILT	24	Resistor at this pin sets the dominant filter cut-off frequency for the filter internal to the chip between IMX± and IDAT pins. A 4KΩ at this pin gives a 3dB point of 8.3MHz.
SHUTDOWN	5	This digital input should be LOW during normal operation. A TTL/CMOS high input on this pin shuts down all the oscillators
TAGC	26	This voltage output can be used to gain control the tuner front-end.
VCC1	3	Supply voltage for front end sections. Usually 12V.
VCC2	23	Supply voltage for the synchronous demodulator and backend sections. Usually 12V.
VCC3	12	Supply for digital logic, prescalers and oscillators. Usually 5V.
VCO1, VCO2	13, 14	The frequency setting network and the varactor are connected at these pins.
XTL1, XTL2	9, 10	Crystal oscillator pins.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Positive power supply, VCC		7	V
Negative power supply, VEE		-7	V
Differential input voltage		10	V
Operating temperature	0	70	°C
Storage temperature	-40	125	°C
Lead temperature (10 seconds soldering)		300	°C
Thermal resistance, Θ_{JA}		90	°C/W
Short circuit tolerance: One output can be shorted to ground.			

Note:

1. Absolute maximum ratings are those beyond which operation and reliability of the device cannot be guaranteed. Subjecting devices to these limits for extended periods of time may result in actual failure of the device.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC1, VCC2	Analog supply voltages	10.8	12	13.2	V
VCC3	HF supply voltage	4.5	5	5.5	V

DC Characteristics

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, AFC_SWT = OFF, T_A = 0 to 70°C unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
ICC – Supply Currents						
ICC1	Front-end Supply Current	VCC1=13.2V		32	40	mA
ICC2	Backend Supply Current	AFC_SW=OFF, AFC_SW=ON, VCC2=13.2		28	34	mA
ICC3	HF Supply Current	AFC_SW=OFF, AFC_SW=ON		16	20	mA
Pw	Total Power Consumption	VCC1,2=13.2V, VCC3=5.5		0.88	1	W
Signals – DC Compliance						
Viout	I-Data Output		4.5	6	7	V
VImix±	I-channel mixer ouput dc		3	4	5	V
δVImix±	I-channel mixer output Differential Offset		-16		16	mV
δAFC±	AFC limiter input Offset	Rs = 2K to 5V.	-4		4	mV
VIoff	Total I-channel Offset		-15		15	mV
ZIout	I-Filter Output impedance			5	10	Ohms
ΔI_{PDO}	PDO charge-pump current swing	PDO to 5V with 10K		±50		mA
δI_{PDO}	PDO charge-pump offset current with offset null over temperature.	Minimized by adjusting 12K variable resistor on Qadj pin.		±200		nA
ΔI_{AFC}	AFC charge pump current swing			±0.6		mA
δI_{AFC}	AFC charge pump offset				±10	μA
I_{OAFC}	AFC charge pump leakage	AFC_SWT=LO			±1.0	μA
I_{VCO1}	VCO external current	VCO1=V_{CC3}		0.5		mA
VCO2	VCO voltage Compliance		0.6		1	V
VX2	Xtal Oscillator Input		2.9		4.9	V
ΔI_{AGC}	AGC charge current swing	Toggle GUP & GDN. Measure current @ 5V		±1		mA
I_{OAGC}	AGC charge pump leakage	G_{UP} & G_{DN} = LO		±125	±250	nA
IF – Signals						
IN±	IF input DC levels			8		V
Rin	Input impedance			3		KΩ
Tagc_hi	Tuner AGC for maximum gain	RLmax=4K,VCC=10.8, VDLY=6V, CAGC=10V		10		V
Tagc_lo	Tuner AGC for minimum gain	VDLY=6V, CAGC=2V		2		V
Tagc_off	Tuner AGC for shutdown	VDLY=6V, CAGC=2-10 SHUTDWN=H	2		10	V
ZTagc	Tuner Impedance during shutdown	VDLY=6V, CAGC=2-10		60		KΩ

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Digital Signal Characteristics for G_{UP}, G_{DN}, AFC_SWT, SHUTDOWN

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, T_A = 0 to 70°C unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Vth	Logic Threshold	VCC3 = 4.5V, 5.5V		1.4		V
HI-VG+	Gain Control Input Logic High	VCC3 = 4.5V, 5.5V	2.4	3.6	V	
LO-VG+	Gain Control Input Logic Low	VCC3 = 4.5V, 5.5V			0.8	V
I(vg)	Logic Input Currents	VCC3 = 4.5V, 5.5V			10	μA

AC Characteristics

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, AFC_SWT = OFF, T_A = 0 to 70°C unless otherwise specified. Refer to Figure 2.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
IF input						
Rin	AC Input imp. @ Max Gain	44MHz	1.5			KΩ
Rin	AC Input imp.@ minimum gain	44MHz	1.5			KΩ
Cin	Ac equivalent input cap			6		pF
NF	Noise Figure @ Max Gain	Rs = 75Ω, 44MHz		8.2	10	dB
Vins	Input Sensitivity @ Max Gain	44 MHz		1000		μVpp
IMD3	Inter-modulation Distortion for two-tone input	VCO=4x46.69, f1/f2=41.69/42.69MHz, Idat=0.7Vpp		-50	-45	dBC
Gain Control Characteristics						
Gmax	IF to baseband max Gain	Vin=-30dBmV@ 44MHz	57	60	63	dB
Ragc	AGC gain range	Vin-30 to +30 dBmV, Cagc=2V to 10V	40	46		dB
Sagc1	AGC sensitivity to gain control at maximum slope	V@ Cagc=8.5V to 9.5V DLYADJ=6V		15	22	dB/V
Sagc2	AGC sensitivity to gain control	V@ Cagc=3.5V to 4.5V DLYADJ=6V		3		dB/V
TPagc	Response time of AGC circuit	From GUP/GDN edge to CAGC current change			20	nS
NF0	Noise figure at no gain reduction	Cagc ≥ 10V, with SAW DLYADJ = 6V		10	12	dB
NF25	Noise figure at 25dB gain reduction	Cagc = 6V, with SAW DLYADJ = 6V			14	dB
NF40	Noise figure at 40dB gain reduction	Cagc = 3C, with SAW DLYADJ = 6V			30	dB
S/N	Signal-to-noise at min. gain	V = 1Vpp, 1MHz	45	47		dB

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AC Characteristics

V_{CC3} = 5V, $V_{CC1,2}$ = 12V, AFC_SWT=OFF, T_A = 0 to 70°C unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
QMDD04 – Quadrature Demodulator						
LO	4 x Demodulating Freq.		100	186.76	250	MHz
BW_Mx	Mixer input bandwidth (+0.1dB)	Over 6MHz bands	30		60	MHz
BW_IFO	IF output from AGC into QDMD		30		60	MHz
DCG	Differential Conversion Gain			10.8		dB
Vo1dB	IMixer Vout @1dB compression	Diff Output, Δf=1MHz		1.5		Vpp
VoqdB	IMixer Vout @ 0.25 dB compression	Diff Output, Δf=1MHz		0.75		Vpp
ephase	I & Q phase error	On-chip	-2		2	deg
I-channel Filtering at Baseband						
APB	Pass Band Attn. @5.8MHz				0.5	dB
f-3dB	-3db Frequency		8.1			MHz
GF	Filter gain Diff In/Single Out			3.5		dB
A90	Attenuation @ IF+LO	see 14.1, (46.69+41.69)	50	54		dB
A46	Attenuation @ 46.69MHz	Vout=1.4Vpp @1MHz		5		mVpp
V_{O1DB}	Ida compression @2Vpp	Diff Output @ 1MHz,			1	dB
V_{OQDB}	Idat compression @0.75Vpp	Diff Output @ 1MHz			0.25	Vpp
FPLL Characteristics						
TSfc	VCO Long Term Stability	fc=186.76MHz,Vpll1=6	fc-500		fc+500	KHz
Svco	VCO sensitivity	fc=186.76MHz,Vpll1=6		400		KHz/V
dVafc±	AFC limiter input beat note	Pilot In = 46.69MHz, IMx±=88mVpp, Vco @ (46.69M±75K)		50		mVpp
DVafc±	AFC limiter input with Crystal ON i.e. AFC_SWT=ON	Xtal @ 46.69MHz Vco @ (46.69M±750K)		100		mVpp
fn	VCO phase noise	At ±20KHz offset			-105	dBC/Hz
BWpll	PLL Bandwidth			2.2		KHz
DIPDO	PLL Output Current Swing			±50		uA
Gpd	Phase Detector Gain	Imix± = 88mVpp, 1KHz PDO connected with 10K resistor to 5V.		4.5		uA/rad
TGpd	PD Gain temperature Coeff.			1000		ppm/K
edc	Static Phase Error due to Prescaler & DC offsets	With Offset Adjust	-4		4	deg
Auxiliary Section (see Figure 1)						
fXCL	Crystal Oscillator Freq	Series , 3rd Overtone		46.69056		MHz
TfXCL	Crystal Temperature Stability	See Figure 1		50		ppm/°C
TXon	Crystal Turn On Time	from AFC_SWT=HI (on)		100		ns
TXon	Crystal Turn OFF Time	frm AFC_SWT=LO (off)		100		ns

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Applications Discussion

System Overview

The RC6516 is used in a Zenith Digital Cable Modem using multi-level VSB formats. The RC6516 performs IF amplification with gain control, synchronous demodulation of I and Q channels and carrier recovery using a Frequency and Phase Lock Loop. The I Channel analog output is digitized in an A/D converter at a rate of 10.76 MHz. The digital data is then used by the Digital Logic IC to perform segment sync recovery, signal polarity correction, symbol clock recovery, AGC and AFC control, channel equalization, phase error tracking, data de-interleaving, Reed Solomon error control and data slicing. (The block diagram of a typical receiver system using RC6516 is shown in Figure 1.

The RC6516 is between a SAW filter and an A/D. The RC6516 output is AC coupled to an 8 bit or 10 bit A/D. An FPLL circuit is used for carrier recovery and synchronous demodulation. A small pilot signal is present in the received signal to aid in carrier recovery. A microprocessor is used to tune the two local oscillators, initialize the system during start up and monitor system performance.

Figure 2 shows the typical external components and connections required for the operation of the RC6516.

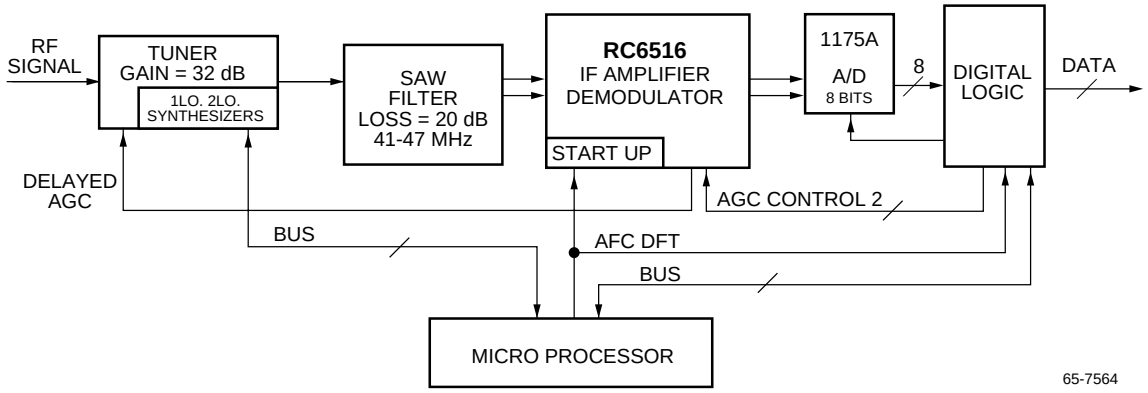

Figure 1. VSB Receiver Front End

Table 2. Signal Levels and Gain Distribution in Receiver Front-End

V_{CC3} = 15V, $V_{CC1,2}$ = 12V, T_A = 0 to 70°C unless otherwise specified.

Parameter	Max. Level	High Level	Mean Level	Low Level	Min Level	Unit
Tuner Input	-28.9	-21.3	-1.3	18.7	23.7	dBmV
Tuner Gain	34	34	33.5	21.4	19.1	dB
SAW Filter Gain (-Loss)	-18	-18	-18	-18	-18	dB
IF Input (Diff-in)	-12.9	-5.3	14.2	22.1	24.8	dBmV
LNA Gain	25.8	25.8	25.8	22.8	20.1	dB
VGA Gain	19.6	12.0	-7.5	-12.4	-12.4	dB
Mixer Input (Diff-in)	32.5	32.5	32.5	32.5	32.5	dBmV
Mixer Input rms	42.2	42.2	42.2	42.2	42.2	mVrms
Mixer Gain	10.9	10.9	10.9	10.9	10.9	dB
Max. Output (Diff-out)	148	148	148	148	148	mVrms
Filter Amp (Diff-in Sng-out) GAIN	3.6	3.6	3.6	3.6	3.6	dB
Iout+ Output (rms)	224	224	224	224	224	mVrms
Iout (peak-to-peak)	1	1	1	1	1	Vpp

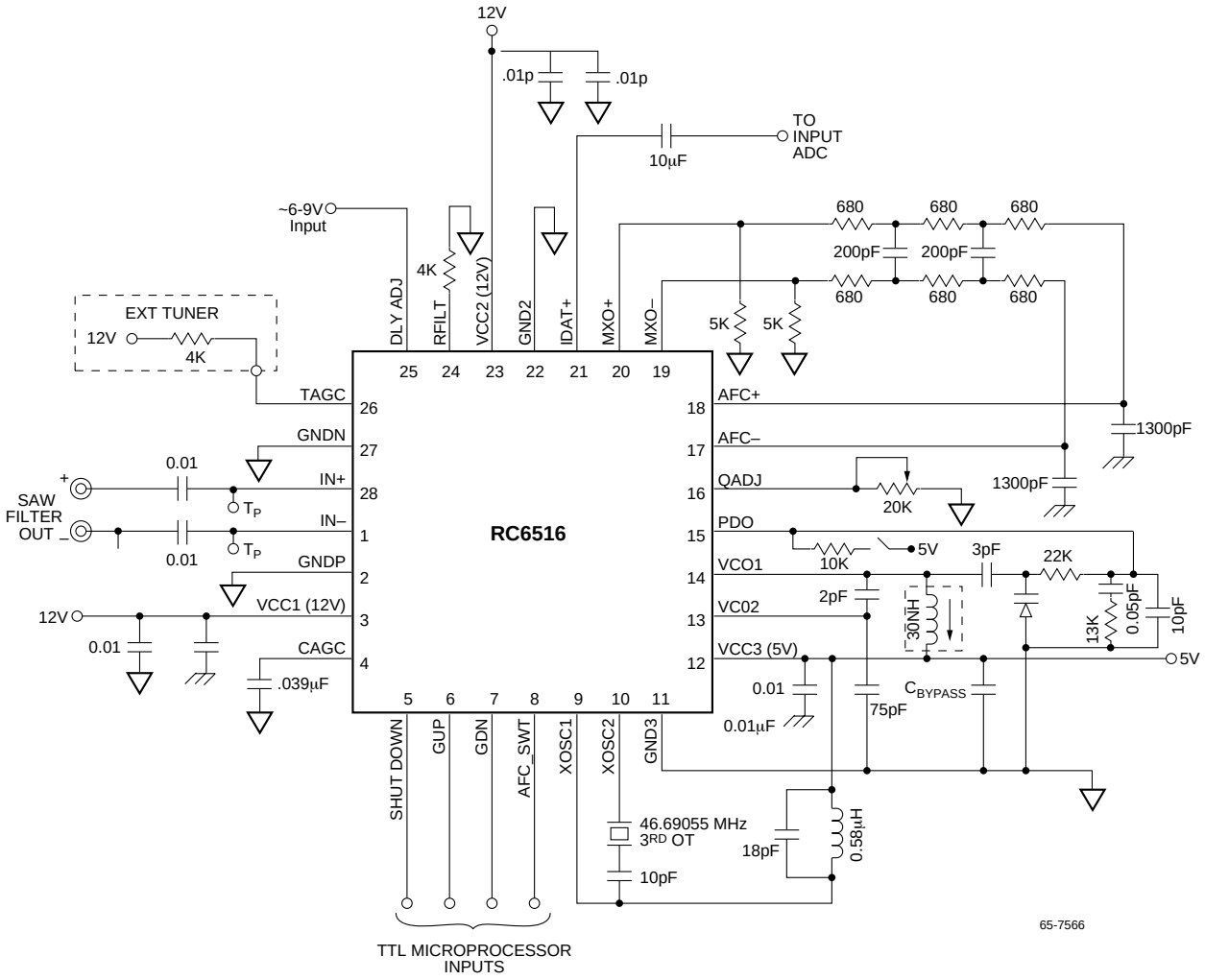

Figure 2. Typical External Components for RC6516

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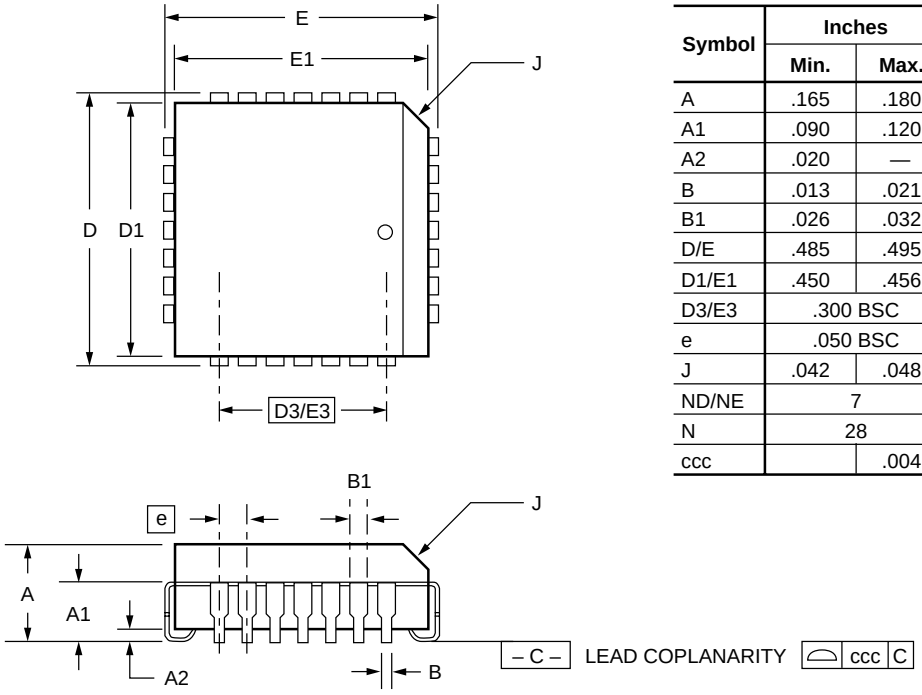
Notes:

Mechanical Dimensions – 28-Lead PLCC (QA) Package



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.04	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	8
ND/NE	7		7		
N	28		28		
ccc		.004		0.10	

Notes:

1. Cavity mismatch = .004 (0.10mm)
2. Cavity frame offset = .002 (0.05mm) excluding leadframe tolerances.
3. Mold protrusions: Parting Line = .006 (0.15mm), Top or Bottom = .001 (0.025mm)
4. Variation in lead position = .005 (0.13mm)
5. Shoulder instrusions & protrusions: Intrusions = .002 (0.05mm), Protrusions = .003 (0.08mm)
6. Package warpage, WARP FACTOR = 2.5 = $\frac{\text{WARP (mils)}}{\text{PACKAGE LENGTH (inches)}}$
7. Ejector pin depth = .010 (0.25mm) maximum.
8. Corner and edge chamfer = 45°C.

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Ordering Information

Product Number	Temperature Range	Screening	Packaging	Package Marking
RC6516	0° to 70°C	Commercial	28 Pin PLCC	RC6516V

5/20/98 0.0m 001
Stock#DS30006516